IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of:	)	Examiner: Idriss N. Alrobaye
Paul L. Master, et al.	)	
	)	Group Art Unit: 2183
Appl. No.: 09/997,530	)	
	)	
Filed: November 30, 2001	)	
	)	
For: APPARATUS, SYSTEM AND METHOD FOR CONFIGURATION OF ADAPTIVE INTEGRATED CIRCUITRY HAVING FIXED, APPLICATION SPECIFIC COMPUTATIONAL ELEMENTS	)	

MS Appeals
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY BRIEF PURSUANT TO 37 C.F.R. § 41.37

Dear Commissioner:

This Reply Brief is filed in support of Appellants' appeal to the Board of Patent Appeals and Interferences ("Board") from the rejection of claims 182-305 in the September 25, 2009 Final Office Action. (Exhibit B).[1] An Answer Brief ("Answer") was submitted by the Examiner dated June 18, 2010 and therefore the due date for this Reply Brief is two months from the mailing date of the Answer i.e., by August 18, 2010 and this brief is being timely filed.

ARGUMENT: THE ANSWER IMPERMISSIBLY DERIVES NON-EXISTENT CLAIM ELEMENTS FROM WISE AND IN SO DOING FAILS TO DEMONSTRATE THAT WISE AND BAXTER ANTICIPATE THE INDEPENDENT CLAIMS

In the initial Brief, Applicants' argued that the combination of Wise and Baxter did not disclose: a) a first and second computational unit each having heterogeneous computational

[1] Applicant will reference Exhibits attached to the initial Appeals Brief.

elements; and b) an interconnection network for configuring interconnections between computational elements in response to configuration information to perform functions.

The Answer continues to misconstrue the Wise reference by adding claim elements that are not disclosed by Wise and would only be possible with impermissible reconstruction using the claim language as a template. Although Wise makes reference to the term "reconfiguration," reconfiguration in Wise is not performed using an interconnection network to configure interconnections between different computational elements as required by the present claims. Wise describes fixed circuits such as the inverse discrete cosine transform (IDCT) block shown in Fig. 137 cited by the Answer that have a limited function because the circuits are fixed. (Ex. C). Such fixed circuits cannot be configured by an interconnection network designed to change (configure) interconnections between the computational elements. The overall architecture in Fig. 137 makes it clear that there is no interconnection network since none of the connections shown between the various adders, subtractors and multipliers may be changed to perform a different function other than a cosine transform.

A. Claims 183, 213, 246 and 276 Are Allowable Because Wise Does Not Disclose A First Computational Unit And A Second Computational Unit

Claims 183, 213, 246 and 276 require a first computational unit having a configurable basic architecture and a second computational unit having a configurable complex processing architecture. Both of these distinct computational units include a plurality of heterogeneous computational elements.

The Answer asserts that the IDCT block in Fig. 137 of Wise shows first and second computational units as the elements having Y inputs (first unit) and elements having X outputs (second unit). (Table, pp. 4-5, 20). The Answer explains that the y inputs have components that include a carry-save multiplier, a carry save adder and a carry save subtractor while the x inputs

have components that include a carry-save multiplier and a resolving adder/subtractor. (pp. 4-5). The Answer also makes the somewhat novel argument that nothing in the claim language prevents a single circuit such as Fig. 137 as being both the first and second computational units. (p. 22).

Applicant maintains that Fig. 137 in Wise shows is a single computational unit and moreover only has a single function. Significantly, the Answer cannot point to any disclosure in Wise that the circuit in Fig. 137 should be construed as anything other than a single computational unit. The Answer ignores the description in Wise of Fig. 137 as the inverse discrete cosine transform (IDCT) block of the code detector. (Ex. C, Col. 259, ll. 35-51). This section does not describe the circuit in Fig. 137 as different discrete computational units, it in fact teaches away from such an interpretation because the entire unit performs the function of an inverse discrete cosine transform.

The Answer has asserted that the column of computation elements in Fig. 137 constitute a first computational unit at the Y input and the column of computation elements at the X output after the common block. (p. 20). The division of a unitary circuit into computational units based on elements is arbitrary and there is no disclosure in Wise that supports such an organization as urged by the Answer. Moreover, none of these asserted computation elements that make up the alleged "computational units" in Fig. 137 are heterogeneous. The computational elements of the Y inputs are all adders while the computational elements of the X outputs are all resolving adder/subtractors. (Ex. C, Fig. 137). Even including components of the common block in Fig. 137 as implied by the Answer does not provide any indication of what would constitute a first computational unit and a second computational unit. One of ordinary skill in the art would not

read Fig. 137 as disclosing two computational units without employing the hindsight of using the claim language as a template.

B. The "Computational Units" In Wise Do Not Have A Plurality Of Computational Elements With Configured Interconnections To Perform Different Functions

The independent claims also require that the first and second computational units each couple a plurality of heterogeneous computational elements together to perform a basic computational function and a complex processing function. The Answer has identified addition or subtraction as a basic function of the first unit (p. 4) and a carry save multiplier or matrix multiplier as a complex computation function of the second unit (p. 5). However, neither of these functions are performed by a plurality of heterogeneous computational elements together as required by the claim language.

The arbitrary organization of components in a unit as asserted by the Answer do not include computational elements which together perform a function. Accepting that the first computational unit include the components coupled to the Y inputs in Fig. 137, the functions of addition and subtraction are performed by single, independent, computational elements such as an adder and subtractor. Each computational element may perform a function, but they do not perform a function together as required by the claims.

This is also true of the alleged "second computational unit" identified by the Answer which are the arbitrary group of components coupled to the X inputs in Fig. 137. (Ex. C). The functions of carry save multiplier or matrix multiplier are performed by single computational elements and not by the computational elements in the second computational units interacting together via the interconnection network. As explained above, Fig. 137 is a single unit

composed of all of the various elements such as multipliers, adders, etc. that work together to perform a single function. It does not perform two functions as required by the claims. The block shown in Fig. 137 is a single computational unit and cannot be separated into two computational units each performing separate functions and therefore does not anticipate these claim elements.

The Answer also newly cites Fig. 141 as disclosing functions for the computational units. (p. 5). Fig. 141 does not disclose two separate computational units and the Answer does not explain how Fig. 141 discloses two computational units. Further, Wise makes it clear the Fig. 141 is a single circuit that performs a single function of 1D transforms. (Ex. C, Col. 262, ll. 55-61).

C. Claims 183, 213, 246 and 276 Are Allowable Because Wise Does Not Disclose An Interconnection Network That Configurably Couples The Interconnections Between Computational Elements In Response To The Configuration Information

All of the independent claims require interconnection networks for each computational unit that each "configurably couple the respective plurality of computational elements" and for "configuring interconnections between" the computational elements in response to the configuration information. The Answer has asserted that Wise shows a "reconfiguration interconnection network as shown in Fig. 137 that reconfigures specific functions." (p. 17). As noted previously, the term "reconfiguration" in Wise relates to selecting predefined functions of various computational elements. Moreover, the reconfiguration in Wise is performed by a separate module that has no relation to the circuit shown in Fig. 137 which is the only disclosure of a computational unit asserted by the Answer. The Answer asserts that "reconfiguration" should be construed as broadly as possible. (p. 17). Regardless of the interpretation of

"reconfiguration," the Answer has still not provided any specification support for either the existence of an interconnection network in Fig. 137 or any disclosure in Wise to support that such an interconnection network configures interconnections between the plurality of computational elements as required by the claims.

The Answer further asserts that the instant application fails to provide a specific or an explicit definition for the term "configuration." (p. 20). A reading of the specification indicates that configuration is accomplished by configuration of the interconnections between the elements themselves in order to change the function of a computational unit (Ex. A, ¶ 41, Spec. p. 13, ll. 10-15) which is precisely the argument that is dismissed without any explanation by the Answer. (p. 20).

Specifically, the interconnection network allows for the configuration of computational elements of a computational unit by changing connections between the computational elements to have the computational unit perform different functions. The specification details this feature as distinct from prior art connections such as bus types:

> In the preferred embodiment, the various interconnection networks are implemented as described, for example, in U.S. Pat. No. 5,218,240, U.S. Pat. No. 5,336,950, U.S. Pat. No. 5,245,227, and U.S. Pat. No. 5,144,166, and also as discussed below and as illustrated with reference to FIGS. 7, 8 and 9. **These various interconnection networks provide selectable (or switchable) connections between** and among the controller 120, the memory 140, the various matrices 150, and **the computational units 200 and computational elements 250 discussed below, providing the physical basis for the configuration and reconfiguration referred to herein**, in response to and under the control of configuration signaling generally referred to herein as "configuration information".

(Ex. A, ¶ 41, Spec. p. 13, ll. 7-15, emphasis added).

The Answer has asserted that the claims do not require a changing of interconnections since all that is required is to configure heterogeneous elements. (p. 25). This is an incorrect reading of the claim language. The claims actually require that the interconnection network

configures interconnections between the computational elements and not configure the elements themselves. Applicant respectfully submits that the common understanding of "configure" in conjunction with "coupling" interconnections as required by the claims requires a change in interconnections. This interpretation is also supported by the specification which is quoted above. More importantly, the configuration of the interconnections in the network must allow the computational units to perform different functions via configuring the interconnections between computational elements.

This differs greatly from Wise where nothing indicates that the interconnection network (the combination block in Fig. 137) is configured in order to change the functions of the computational units as asserted by the Answer. (p. 25). The Answer argues that the common block in Fig. 137 may perform to configurably couple the components of the Y-inputs to perform different functions, but does not explain how configuration of the interconnection network changes between these different functions. (p. 25).

The Answer has explained that Fig. 137 of Wise as disclosing such an interconnection network. (pp. 4-5). The Answer further clarifies by noting that Col. 12, ll. 45-47 disclose a reconfiguration to specific function. (pp. 18-19). As Applicants have noted in their initial Brief, nothing in Wise indicates how Fig. 137 itself could be reconfigured based on a two line snipet occurring almost 240 columns before in the Wise patent specification. In fact, Col. 12, ll. 45-47 of Wise is part of a glossary of terms which have no relation to the actual sections noted by the Answer. (Ex. C). Specifically, this defines a reconfigurable process stage (RPS) as "a stage, which in response to a recognized token, reconfigures itself to perform various operations." (Ex. C, Col. 12, ll. 45-47). There is nothing in Wise or in the Answer that indicates that Fig. 137 or Fig. 141 is a reconfigurable process stage and therefore there is no support that Fig. 137, the only

circuits referenced by the Answer that could be configured to perform a functions. Further, there is nothing in even Col. 12, ll. 45-47 of Wise that indicates that the configuration occurs via an interconnection network configuring interconnections between computational elements as required by the claims. The only sections in Wise that explain the RPS is Col. 52, l. 20 to Col. 55, l. 34. (Ex. C). Nothing in this section indicates that the reconfiguration is accomplished by configuring interconnections between computational elements as required by the claims.

The Final Office Action has not provided any explanation of what elements in Fig. 137 constitute an interconnection network, let alone a network that may configure the interconnections between the computational elements. An examination of Fig. 137 shows that the connections between the various adders, multipliers and subtractors are permanent wired connections and therefore the connections cannot be changed or configured. Further the connections are more akin to a bus rather than a true network that may route data between each computational elements. Even if certain routing may be performed via latches, the set of connections is fixed and data may only be routed to certain computational elements. The configuration in Fig. 137 therefore is not a network because it cannot configure the interconnections between the computational elements. Since Wise does not disclose an interconnection network, let alone one which changes the interconnections between the computational elements, Wise does not anticipate the pending claims.

CONCLUSION

For at least the foregoing reasons, the final rejection of appealed claims 183-305 set forth in the Final Office Action mailed September 25, 2009, should be reversed.

Respectfully submitted,

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